IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of Robert J. Falster et al.
Serial No. To Be Assigned
Filed February 11, 2002
For   THERMALLY ANNEALED, LOW DEFECT DENSITY SINGLE CRYSTAL SILICON

February 11, 2002

PRELIMINARY AMENDMENT A

TO THE ASSISTANT COMMISSIONER FOR PATENTS,

SIR:

Please enter the following amendments.

IN THE TITLE:

Please replace the title with the following new title: "THERMAL ANNEALING PROCESS FOR PRODUCING LOW DEFECT DENSITY SINGLE CRYSTAL SILICON."

IN THE SPECIFICATION:

Please replace the paragraph beginning at line 3, page 1 with the following rewritten paragraph:

CROSS-REFERENCE TO RELATED APPLICATION

This patent application claims priority from U.S. Provisional Patent Application Serial No. 60/104,304 filed on October 14, 1998, and U.S. Serial No. 09/416,998, filed on October 13, 1999.

IN THE CLAIMS:

Please cancel claims 1-18.

IN THE ABSTRACT:

Please replace the text in the abstract beginning on page 66, line 1 with the following rewritten text:
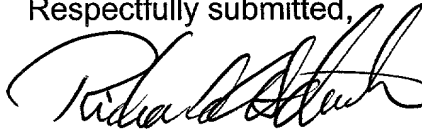
A thermal annealing process for producing a low defect density single crystal silicon wafer. The process includes thermally annealing a wafer having a first axially symmetric region which extends radially inwardly from the circumferential edge, contains silicon self-interstitials as the predominant intrinsic point defect and is substantially free of agglomerated interstitial defects and a second axially symmetric region which has vacancies as the predominant intrinsic point defect. The wafer is subjected to a thermal anneal at a temperature in excess of about 1000°C in an atmosphere of hydrogen, argon or a mixture thereof to dissolve agglomerated vacancy defects present in the second axially symmetric region within a layer extending from the front side toward the central plane.

REMARKS

This application is a divisional application based on U.S. Application Serial No. 09/416,998 filed October 13, 1999. Claims 1-18 were elected in the parent application in response to a restriction requirement, and were allowed on November 5, 2001. Accordingly, claims 1-18 are hereby cancelled from the present application. Claims 19-40 are now pending in this application. Attached hereto is a marked-up version of the changes to be made to the application, entitled **"Version With Markings To Show Changes Made"**.

Applicants also enclose herewith a check in the amount of $776.00 to cover the filing fee for this application. The Commissioner is hereby authorized to charge any deficiency or overpayment in connection with this application to Deposit Account No. 19-1345.

Respectfully submitted,

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RAS/msc
*Attachment/Enclosure

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<u>VERSION WITH MARKINGS TO SHOW CHANGES MADE</u>

<u>IN THE TITLE</u>:

The title has been amended to the following:

THERMAL[LY] ANNEAL<u>ING</u>[ED,] <u>PROCESS FOR PRODUCING</u> LOW
DEFECT DENSITY SINGLE CRYSTAL SILICON

<u>IN THE SPECIFICATION</u>:

The paragraph beginning at line 3, page 1 has been amended to the following:

CROSS-REFERENCE TO RELATED APPLICATION

This **patent** application claims priority from U.S. **P**[p]rovisional **Patent**
A[a]pplication Serial No. 60/104,304, filed on October 14, 1998 **and U.S. Serial No.**
09/416,998, filed on October 13, 1999.

<u>IN THE CLAIMS</u>:

Claims 1-18 have been canceled.

<u>IN THE ABSTRACT</u>:

The Abstract text beginning at line 1, page 66 has been amended as follows:

A **thermal annealing process for producing a low defect density** single
crystal silicon wafer**[having a central axis, a front side and a back side which are**
generally perpendicular to the central axis, a central plane between the front and
back sides, a circumferential edge, and a radius extending from the central axis
to the circumferential edge. [The wafer comprises first and second axially
symmetric regions]. The **process includes thermally annealing a wafer having a**
first axially symmetric region **which** extends radially inwardly from the circumferential

edge, contains silicon self-interstitials as the predominant intrinsic point defect, and is substantially free of agglomerated interstitial defects[. The], a second axially symmetric region **which** has vacancies as the predominant intrinsic point defect[, **comprises a surface**]. **The wafer is subjected to a thermal anneal at a temperature in excess of about 10000°C in an atmosphere of hydrogen, argon or a mixture thereof to dissolve**[layer extending from the front side toward the central plane and a bulk layer extending from the surface layer to the central plane, wherein the number density of] agglomerated vacancy defects present in the **second axially symmetric region within a layer extending from the front side toward the central plane**[surface layer is less than the concentration in the bulk layer].